

HYBRID METAL-SEMICONDUCTOR STRUCTURES BASED ON InP AND GaAs NANOTEMPLATES FOR ELECTRONIC AND PHOTONIC APPLICATIONS

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PhD Thesis Summary

Abstract. In this scientific work are presented the results that contribute to solving an important scientific problem related to obtaining of porous templates with controlled morphology and design by replacing acidic and alkaline electrolytes, the use of which presents a danger for the environment, with neutral electrolyte (NaCl) as well as obtaining of the metal-semiconductor hybrid structures using pulsed electrodeposition that offers additional possibilities to control the localized deposition in certain portions of the porous template and allows the controlled fabrication of nanodots, nanowires, nanotubes and perforated metal nanomembranes. Mechanisms of pore propagation in InP and GaAs semiconductor substrates and electrochemical deposition of metals in the produced porous templates are identified and discussed, which allowed to control the direction of pore growth, including those parallel to the substrate surface as well as localized Au deposition.

Keywords: Electrochemical Etching, Current Line Oriented Pores (CLO), Electrodeposition, Pt Nanotubes, Gold Nanomembranes.

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1. Introduction. Motivation of the study

Increased attention to a class of nanostructured materials, namely porous layers, was paid after the discovery of luminescence in porous Si by Canham in 1990 [1], due to the introduction of pores by the electrochemical method by Lehman and Goesele [2]. Electrochemical etching of semiconductor substrates is widely used in the fabrication processes of semiconductor nanostructures [3]. The formation of porous layers by electrochemical methods has been studied quite extensively over three decades, the results being systematized in the monographs of Zhang [4] and Lehman [5].

Semiconductor compounds offer more possibilities for applications in optoelectronics and photonics due to their wider bandgap. Analysis of the literature shows that III-V semiconductor compounds have been extensively studied for the

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introduction of porosity by anodization. A wide variety of morphologies obtained due to the diversity of the chemical composition of III-V semiconductor compounds compared to porous Si have been reported in review articles by Prof. Föll and colleagues in 2003 [6] and 2010 [7]. Later, II-VI semiconductor compounds were also subjected to electrochemical nanostructuring, the results being compared with those of III-V semiconductor compounds and systematized in the review paper [3].

Formation of hybrid metal-semiconductor structures is also being intensively researched due to their remarkable properties that are not characteristic of the materials used separately [3]. In the case of semiconductor substrates, metal filling can be performed by electrochemical deposition, which is a cost-effective method.

The water crisis is likely to worsen in the coming decades, prompting research teams to develop low-cost water purification technologies with minimal chemicals to reduce further environmental pollution [8]. However, there is a trend towards developing green technologies for the production of nanostructured materials that do not harm the environment.

Formulation of the scientific problem based on the study of scientific literature in the field of study

The reviewed literature in chapter 1 provides a strong foundation for formulating significant scientific problems in nanotechnology. Addressing these challenges will lead to the development of novel materials, devices, and technologies with impactful applications across various fields.

Semiconductor templates have demonstrated essential advantages over other types of templates such as dielectric ones that would allow a higher applicability in nanotechnological processes through the formation of hybrid structures due to the deposition of metals inside the pores. The electrical conductivity of the porous skeleton from the semiconductor templates allows one to obtain nanotubes without additional processes of activation and sensitization of the walls that lead to contamination of the deposited material.

Despite the fact that InP and GaAs semiconductor compounds are similar in terms of parameters, pores oriented along current lines have not been observed and reported in GaAs, which would allow the formation of ordered porous structures.

The morphologies of the porous structures reported in the specialized literature allow to control the direction of the pore growth in depth by the consecutive change of the applied potential from higher values to lower values, which leads to the transition from current line oriented (CLO) to crystallographically oriented (CO) pores [9]. Using the previously developed technology aiming the control of the propagation of pores parallel to the surface, by changing the geometric shape of the photolithographic mask and taking into account the property of CLO pores not to

intersect with each other, it will be demonstrated the self-arrangement of pores in a restricted space forming spectacular morphologies.

Pulsed electrochemical deposition is suitable for deposition in porous semiconductor templates, especially for those with pore diameters smaller than 100 nm, since it is difficult to achieve uniform deposition inside the pores in the case of classical direct voltage or current deposition, requiring a careful optimization of the pulse parameters to achieve this goal.

Typically, semiconductor nanowires are fabricated using growth methods that involve high temperatures and various carrier gases. Unfortunately, these methods can introduce contaminants into the nanowires during growth, ultimately degrading their properties.

The goal of the PhD thesis consists in the comparative study of the electrochemical etching of *n*-InP and *n*-GaAs semiconductor substrates, the optimization of the anodization process for nanostructuring in neutral electrolyte (NaCl) and harmless to the surrounding environment, the examination of the possibilities of obtaining CLO pores in GaAs, the formation of metal-semiconductor hybrid structures with the identification of their fields of application.

To achieve this goal, the following objectives were formulated:

- optimization of the electrochemical etching of the *n*-InP and *n*-GaAs semiconductor substrates in NaCl electrolyte, comparison with anodization in HCl and HNO₃ electrolytes;
- controlling the direction of pore growth in InP templates and localized gold deposition by means of electrochemical methods;
- fabrication of GaAs nanowire networks by anodization of the *n*-GaAs semiconductor substrates; the study of the influence of the type of electrolyte and anodization voltage on the obtained morphology; contacting the individual GaAs nanowire and photoresponse study;
- optimization of the electrochemical deposition process inside the templates based on semiconductor compounds; elaboration of the cost-effective approaches for a controlled deposition on the surface as well as in certain segments of the depth.

2. Techniques used for obtaining and characterization of the nanostructured materials

Chapter 2 describes the main techniques such as electrochemical etching and pulsed electrochemical deposition used to obtain porous layers, as well as metal nanotubes and nanowires. Increased attention is paid to the optimization of the electrochemical cell design. Technological factors such as the influence of the

reaction gas, the distance of the counter electrode from the surface, and the temperature of the electrolyte were excluded by developing the optimized design of the electrochemical cell.

The schematic representation of the elaborated electrochemical cell and used in the thesis, not only for the electrochemical nanostructuring of InP and GaAs crystals, but also for the pulsed electrochemical deposition of metals is presented in Figure 1 [10].

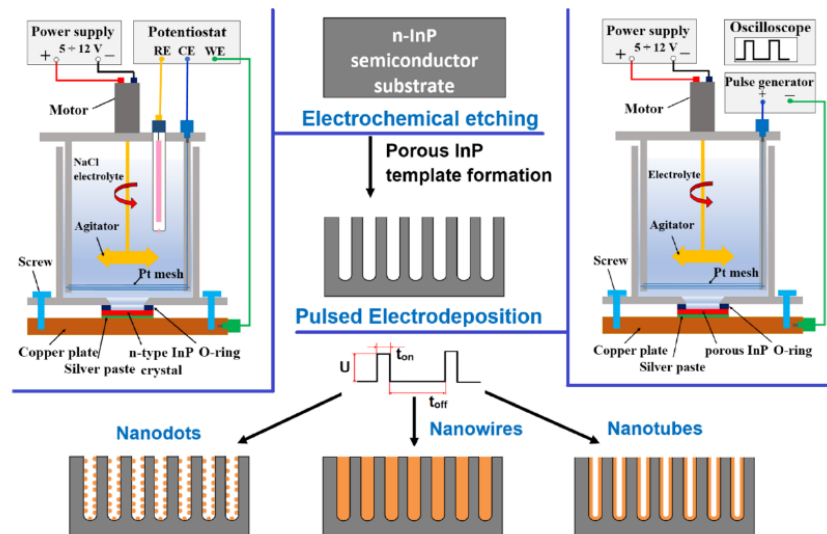


Fig. 1. The schematic representation of the equipment and steps involved in a technological approach for hybrid metal-semiconductor nanostructures obtaining in *n*-InP crystals. The approach consists from electrochemical etching to form pores in the InP, followed by pulsed electrochemical deposition to precisely place the metal structures within these pores [10].

Also in this chapter, the used materials in the thesis are described in detail. Techniques such as classic photolithography, laser photolithography and heat treatment in a controlled atmosphere were also used for the realization of the thesis. Apart from technological approaches, SEM, EDX, XRD and photoluminescence techniques, used for the characterization of the elaborated materials, are described.

3. Development of technologies for obtaining of semiconductor nanostructures with controlled morphologies based on InP and GaAs in neutral electrolyte

In chapter 3, technologies for semiconductor nanostructures obtaining of *n*-InP and *n*-GaAs in neutral electrolyte (NaCl) with controlled morphology were elaborated [11,12]. The comparative study of InP anodization in HCl and NaCl electrolytes demonstrated a similar behavior for both types of electrolytes [13]. The pore

diameter of InP can be changed in the range of 150 nm to 40 nm by changing the concentration of NaCl electrolyte from 1 M to 5 M at the applied voltage of 6 V, being determined as the optimal voltage for the hexagonal packing of the pores that leads to the self-ordering.

An important aspect of this chapter consists in the fabrication of porous *n*-InP layers by design with the involvement of photolithography processes [14]. It was demonstrated that the optimization of the process of obtaining pores parallel to the surface in *n*-InP crystals, by applying the photolithographic mask in the form of a square with the dimensions of the sides of 25 μm (see Figure 2a), it leads to the formation of some spectacular morphologies due to the anodization from all four sides of the mask and the particular self-organization process of the pores oriented along the current lines in the limited space under the photolithographic mask (see Figure 2b). It has been established that the shape of patterns and geometric dimensions defined by the mask play a crucial role in determining the final form of the anodized structures [15].

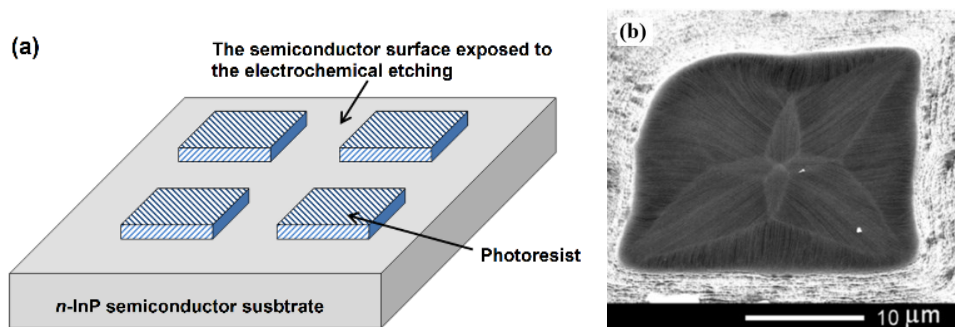


Fig. 2. a. Schematic representation of the mask design used for etching. SEM images of the InP sample surface after electrochemical etching using the square mask approach in (a): **b.** Top view after removing the photoresist layer [15].

It is reported that pores propagating in the direction perpendicular to the crystal surface were obtained using *n*-GaAs crystals with (111) orientation anodized in 1.75 M NaCl electrolyte at anodization voltage of 3 V on the (111)B surface, while the anodization under the same technological conditions on (111)A surface leads to the formation of tilted pores to the crystal surface and intersect each other [16].

Also in this chapter, the formation of GaAs nanowires obtained by electrochemical etching in a single technological step of *n*-GaAs substrates is elaborated and reported (see Figure 3a). The nanowires are oriented perpendicular to the surface, due to the use of substrates with the crystallographic orientation (111)B. The nanowires are characterized by a triangular cross-section having a cross-sectional size of about 400 nm and a length of 100 μm , having an aspect ratio of 250 [12].

Moreover, the formation of diameter-modulated GaAs nanowires by one-step anodization of (111)B-oriented GaAs substrates was demonstrated [15]. The proposed approach is based on anodization at the optimized applied potential, favoring the simultaneous growth of perpendicularly oriented and tilted crystallographic pores on the GaAs surface. The modulation of the diameter of the GaAs nanowire is due to the intersection of these pores. A selective modulation of the nanowires by anodization at two different applied potentials is demonstrated [15].

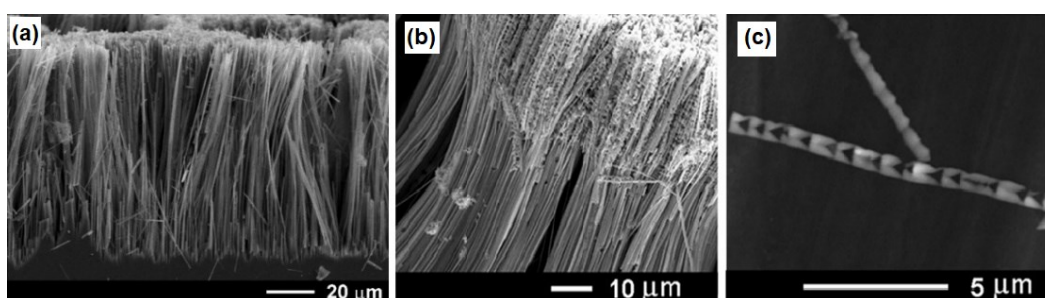


Fig. 3. **a.** Cross-sectional SEM image of a (111)B GaAs sample anodized at 3 V for 20 min in 1 M HNO_3 electrolyte [12]. **b.** SEM image of segmented GaAs nanowires: at the beginning of anodization, a potential of 4.7 V is applied, then electrochemical etching is performed at the anodization voltage 4 V resulting in the formation of smooth GaAs nanowires [15]. **c.** SEM image of the individually perforated GaAs nanowire [15].

In order to expand the application area of the fabricated GaAs semiconductor nanowires, their transformation into gallium oxide by thermal treatment was demonstrated in this chapter. An optimization of the heat treatment process consisting in oxidation at 900 °C in argon flow with a reduced oxygen content (3%) allows to selectively transform GaAs nanowires into Ga_2O_3 with a wide band-gap ($E_{\text{gGa}_2\text{O}_3}=4.9$ eV), being attached on a non-oxidized semiconductor substrate with a narrow band-gap ($E_{\text{gGaAs}}=1.42$ eV) [15].

The applicability of the elaborated GaAs nanowires as a photodetector in the IR spectral range was demonstrated by contacting a single GaAs nanowire via laser beam lithography [12].

4. Hybrid metal-semiconductor nanostructures. Controlled deposition of metal in semiconductor templates

Chapter 4 reports the optimization of pulsed electrochemical deposition parameters, used to obtain hybrid metal-semiconductor structures based on the developed porous nanotemplates.

At the beginning of the chapter, the technology of electrochemical pulse deposition of Au and Pt in desired regions of the porous InP templates was optimized. The

optimization includes the following parameters of the applied pulse: pulse duration (t_{on}); pause between pulses (t_{off}); and the value of the applied voltage (U) (see Figure 1) [2]. It was experimentally determined that a uniform deposition of platinum along the entire length of the pores, which facilitates obtaining metallic nanotubes, can be achieved at pulse parameters optimized from the point of view of efficient electrolyte refreshment and avoiding its depletion in the pores [10].

Reducing the duration between pulses from 1 s to 10 ms leads to the deposition on the surface of the sample and at the same time the contacting of the Pt nanotubes deposited in the first step inside the semiconductor template. The identification of the possibility of the controlled deposition at certain depths of the metal in semiconductor templates was applied for the fabrication of the upper electrical contact in the varicap (variable capacity) device fabricated on the basis of porous GaP template with Pt nanotubes [15,17]. The technological process consists from 2 stages of pulsed electrochemical deposition, in the first stage uniform Pt nanotubes are deposited inside the porous GaP template with a depth of 70 μm , applying the pause between voltage pulses $t_{\text{off}}=1$ s, followed by the second stage of deposition of the upper contact, setting the pulse parameters in such a way as to guarantee the depletion of the electrolyte inside the pores ($t_{\text{off}}=10$ ms) and the deposition of the metal only on the surface [15].

Self-ordered hybrid metal-semiconductor structures have been proposed to be used as planar lenses for photonic applications, the technological realization being demonstrated by two cost-effective designs. The first approach consists of metal coating by pulsed electrochemical deposition on InP semiconductor template walls. In cross-sectional examination by SEM, rows of platinum nanotubes surrounded by semiconductor InP material were observed, being prospective for application as integrated lenses by cleavage of a certain number of rows of such layered hybrid material [11]. The focusing properties can be controlled by adjusting the morphology of the hybrid structures, namely the pore shape, diameter and thickness of the porous template, as well as the deposited metal. The second approach involves the functionalization of semiconductor nanowires with a continuous metal layer, resulting in the formation of core-shell metal-semiconductor structures [10].

At the end of chapter 4, a cost-effective electrochemical technology in two steps at room temperature is demonstrated, which ensures low energy consumption, with simple to operate and cheap equipment for the production of suspended Au nanomembranes, according to the schematic representation in Figure 4 [18].

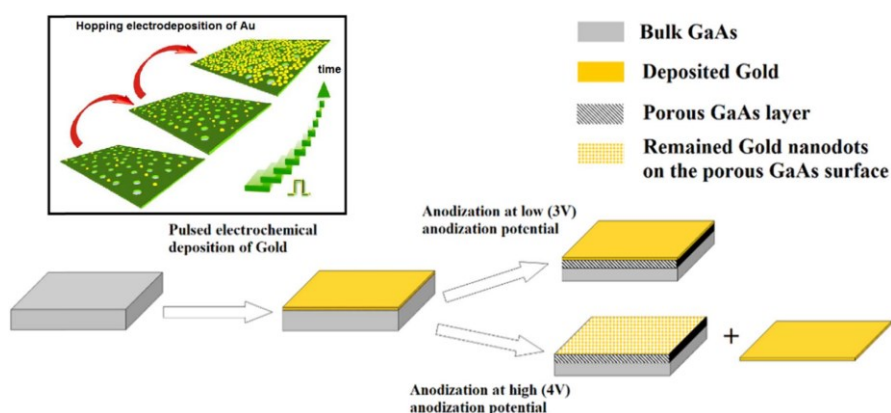


Fig. 4. Schematic representation of the technological process for the fabrication of the Au nanomembrane on a porous semiconductor substrate with the possibility of transfer to another substrate [18]. The inset shows the hopping electrodeposition mechanism of a monolayer of Au nanodots [19].

The deposition of a nanogranular Au thin film (less than 100 nm) on a GaAs semiconductor substrate during the first deposition step is controlled by the "hopping electrodeposition" mechanism [19], which leads to the formation of a monolayer of Au nanoparticles with an average diameter of approximately 20-30 nm (see inset in Figure 4). By varying the duration of the cathodic voltage pulses during the deposition, it is possible to introduce nanopores into the Au film, the diameter of which is adjustable by the duration of the pulse in the range from tens to hundreds of nanometers. The porous nature of the Au nanofilm provides its electrolyte permeability for the second step of the technology, which consists of anodic etching of the semiconductor substrate and the formation of a porous GaAs layer.

Free-standing Au nanomembranes can be obtained by detaching an Au nanomembrane from the porous GaAs layer, which occurs when the anodization voltage above the threshold value of about 4 V in the case of electrochemical etching of GaAs substrates with a free electron concentration of $2 \times 10^{18} \text{ cm}^{-3}$ in 1 M HNO_3 electrolyte [18]. The possibility to transfer the prepared nanomembranes to different substrates makes them promising for potential hetero-integration with advanced optical, plasmonic and electronic systems for new applications.

Conclusions

The scientific problem related to obtaining porous semiconductor nanotemplates by replacing acid and alkaline electrolytes contributes to the development of green technologies for obtaining semiconductor nanotemplates that can be applied in flat photonic lenses by forming metal-semiconductor hybrid structures. Controlling the pore diameter and the thickness of the walls between the pores in the InP

semiconductor nanotemplate allows one to control the diameter of the metal nanotubes and the distance between them, which are important parameters for the focusing properties of photonic lenses. Also, within the framework of solving this problem, the manufacturing of porous n-InP layers by design was demonstrated, taking as a basis the technology previously developed [20], but with the introduction of essential optimization consisting in changing the shape of the photoresist mask from strips to squares.

The scientific problem related to the identification of the possibilities of obtaining pores oriented along the current lines in GaAs, which are parallel to each other, has been partially solved, the final result of the morphology being obtained by mimicking CLO pores in GaAs by selecting the right crystallographic orientation of the n-GaAs substrates and the optimization of electrochemical parameters. The scientific novelty of the obtained results consists in the development and optimization of the technology for the formation of n-GaAs nanotemplates by electrochemical etching in NaCl electrolyte.

In solving the problem related to obtaining metal-semiconductor hybrid structures, it was demonstrated that the use of pulsed deposition offers additional possibilities to control the localized deposition in certain portions of the porous template, which allow the controlled obtaining of nanodots, nanowires, nanotubes and perforated metal membranes.

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