Parity analysis of convergent fan-out signals for the Schneider's counterexample digital circuit

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Abstract - The digital circuit, DC, of the counterexample Schneider [3] was used as a logic structure to which it was demonstrated the insufficiently of the sensitization method for one way (DALG-I) [1], for discovering the error 6≡0 and the argument for elaborating DALG-II [2]. In [4] it's proven that the efficiency of DALG-II was demonstrated for a possible specific error. The results of the testability estimation for this circuit [5] come with a doubt for the correctness of the structure and for the efficiency DALG-II for detecting 6≡1.
Key words: parity analysis, digital circuits, counterexample Schneider, DALG-I, DALG-II

INTRODUCTION

The complexity growth for the digital circuits (DC) involves grater and grater problems, not only for the test generation, but also for the organization of proper testing. In the '60s, this lead to the apparition in the testing area to a new direction – design for testability (DFT). But the fundaments of the testing at that time weren't yet defined: in 1966 Roth elaborates DALG-I, the first algorithm for the elaboration of tests based on the sensitization for a unique way through DC [1]. In 1967 Schneider, presents a DC with the quality of a counterexample [2], which indicates a certain error, undetected by the DALG-I and he also indicates the test which detects the respective error. Roth and Schneider elaborate DALG-II [3], demonstrating the efficiency of this one for a single error (conform to [4]). Except for the suspicion in [4], this raised other questions [4, 5]. The present paper continuous the development of the results in [5] with the parity analyze and a study of the functional and logic properties of a Schneider DC counterexample.

1. BASIC CONCEPTS AND DEFINITIONS

An analysis for the logic properties of a DC presumes an analysis for the parity of the structure and an analysis for the logic properties of the DC's gates, especially for the logic gates with inputs for the convergent fan-out signals. Certain properties of a DC, like the number of logic gates, the type of the logic gates used or the fan-out gates with even and odd number of logic gates until the entrance to the logic convergent gates of the fan-out, also influences the properties for the logic gates of the DC. Still an estimation analysis of the controllability indices and of the observability permits to establish only the structural properties of a DC and can indicate only the potential risks of apparition of logic unsolvable conflicts. A more profound study of this information may be obtained from a study of the functional properties of a DC.

1.1. Properties of the logic signals and gates

There are relationships between the logic values of the inputs of a gate and the outputs. For example, the logic value 0 applied at a single entrance of a AND (NAND) gate causes in a univocal way the logic value 0 (1) at the exit of the gate. In a similar way, the logic value 1 applied at a single entrance of an OR (NOR) gate causes at the exit in a univocal way, the logic value 1 (0). This logic value of the input which on its own, no matter the other values of the inputs from the rest of the entrances of the gate, causes in a univocal way the logic value from the exit of the gate and it's named *dominant logic value (blockage)*. We will mark the dominant logic value on the connection i with ${}^{i}d$. The unique logic value for the output of a gate, which differs from all the others logic values at the exit of this gate, is called *equivalent logic value (sensitization)*. For the AND (NAND) gate the equivalent logic value for the exit signal is 1 (0). In a similar way, for the OR (NOR) gate the equivalent logic value for the exit signal is 0 (1). We will mark with ${}^{i}e$ the dominant logic value on the connection i.

The stimulant vector for the input, to which the equivalent logic value corresponds, is named *equivalent set* of the digital signals values. The logic value of each binary variable from the equivalent set is called *the equivalent logic value of an entrance signal of the gate*. For example, for the AND, NAND, NOR, NOR-NOT an equivalent input set is 111. As a result, 1 is going to be the equivalent logic value of the input for these gates. In opposition, for the gates NAND, NAND-NOT, but also for the logic gates NAND, the equivalent set of input values is 000. The equivalent set has the next properties:

1) Each component of the equivalent set represents a potential logic value for the manifestation for this type of error $i \equiv d$ and the univocal propagation of the correct or erroneous signal to the exit of the gate;
2) The equivalent set $ee..e$ has maximum capacity of detect ability: it can detect singular errors of the kind $i \equiv d$, for the signal from any input

connection – so only a stimulus vector can detect the errors of the $i \equiv d$ kind for all the inputs of the logic gate;

3) The equivalent set detects the presence of one or multiple errors at the inputs of the gate, but it doesn't locate a certain defect entrance. This is one of the properties for the logic gates and there aren't other ways, except for the ones that modifies the structure (auxiliary check up points or auxiliary logic) to overcome this situation. The detected errors from the equivalent set of the stimuli vector for the input values are called equivalent errors.

For the logic gates: XOR, NXOR, SUMM MODULO 2, NOT SUMM MODULO 2, these represent special functions and can use as an equivalent logic value, no matter which of the logic values 0 or 1.

1.2. Functional properties of a DC

In general the logic functional properties of a DC depend on the structural properties of the DC:

1) ways of fan-outs signal conduction through an even or odd number of logic gates until the entrance in the convergent gates;

2) the logic properties for different types of logic gates, thorough which the convergent fan-out signals are propagated; 3) the logic type of gates for the convergences of the signals. In the general case, the functional properties of a DC represent the result of the interaction between the divers' logic gates. A homogenous logic circuit (for example, built only from only one type of logic gates OR or AND) degenerates in the respective logic gate, not having interactions between gates that could change the logic function, and as a consequence, the functional properties correspond in this case with the ones of the logic gate. In the next part we will use the notions and the definitions from [5], and if it is a necessity, are going to be introduced new notions. The total of the logic gates, in function of their properties not to inverse the input, to inverse it or to inverse it in certain cases, can be devised in 3 groups:

1) Logic gates without inverter, for example : AND, OR;
2) Logic gates with inverter at the entrance or at the exit, for example: NAND, NOR, AND-NOT, OR-NOT;
3) Logic gates which, depending of the logic input value at the gate – 0 or 1, will work as a repeater or as an inverter for the other input of the gate, for example: XOR, XOR-NOT.

The number of inversions, which are applied on a logic signal through his logic gates in DC, characterizes the parity of the logic signal on the exit connection compared to his parity on the initial connection. The parity of a logic signal can be odd or even depending on the odd or even number of inverters through which it was propagated. So, the even parity (odd) corresponds to any even number (odd) of inversions. Rightly speaking, from the test generation point of view, not the inversions number of the digital signal is important, but the direct or inversed form of the signal compared to the input form on the initial connection of the considered way. In the case for the same parity on the exit connection and on the entrance connection, the digital signal will have even parity. In the case which the signal appears at the starting point in direct form (inversed), and at the final point in the inversed (direct) form, this signal will have odd parity.

From the test generation point of view there is an interest not only in the parity of the signals at the convergent inputs of the gate, but also in the type of convergent logic gate for the digital signal. The type of convergent logic type of a signal is important, because each gate has its own blocking characteristics (dominant – d) and for activation (equivalent – e) of the ways for each gate. It's significant the fact that only one blocking signal (dominant) blocks the logic gate, no matter what the values of the others inputs. Also, changing the value for that certain input with an equivalent logic signal, it will unlock the gate, inverting the value of the output and being possible the sensitization for all the ways of the gate.

2. THEORETIC ASPECTS OF THE PARITY ESTIMATION FOR THE CONVERGENT FAN-OUT SIGNALS OF A DC

The problem that appears in the case of fan-out convergent consists in the fact that the signals that are propagate through the circuit can appear at the gate convergent entrances in *opposite phase*. This property of the convergent fan-out signals together with the logic properties of the convergent gate, may lead to major problems of test generation, and other times to the impossibility of the test generation. The theoretic aspect of the enounced problem may be shortly exposed in the following way. Assuming, that on the initial connection the signal is in the positive way (the logic signal level is 1) are obtained the next cases.

1) Convergent gate of the type AND, NAND

a) Even parity of the signals on all inputs.

In this case at all the gate convergent entrances there will be the values 11…1, which leads to the sensitization of any way through the gate. But in the case, that on the initial connection the signal will have the value 0, at the inputs of the convergent gate will be applied the set 00…0, which will "profoundly" block the gate NAD or NAND.

b) Odd parity of the signals:

In this case at all the inputs of the convergent gate there will be the values 00…0, which contributes at the blocking of no matter which way through the gate. This is an unsolvable situation for test generation. In the case that on the initial connection the signal will have the value 0, at the gate convergent entrances will be applied the set 11…1, that contributes at the sensitization of no matter what way through the gate;

c) Even parity for some inputs and odd parity for the rest of the inputs.

In this case at some of the inputs of the convergent gate will have the value 0 and others 1, which leads to unsolvable logic conflicts. In the case of the 0 signal on the initial connection the situation remains with a problem.

2) The convergent gate of the type : OR, NOR

a) Even parity of the signals on all inputs.

In this case the inputs at the convergent gate will have the values 11…1, which leads to the blocking of all the ways through the gate, unsolvable situation for the test generation. In the case of the 0 signal on the initial connection at the convergent inputs it's going to be obtained the set 00…0, which allows the sensitization of all the ways through the circuit.

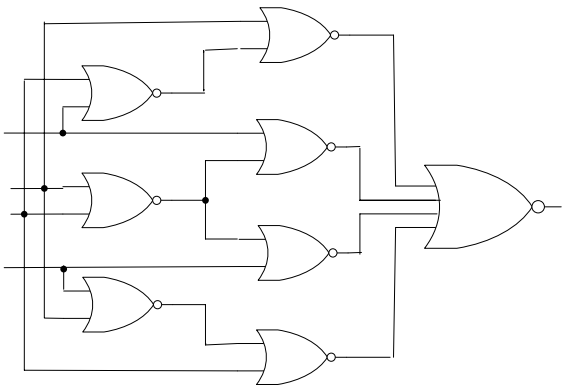

Fig. 1 Digital Circuit of Schneider counterexample

b) Odd parity of the signals:

In this case all the inputs of the convergent gate will have the values 00…0 and this contributes to the sensitization of any way through the gate. In the case of the 0 signal on the initial connection at the convergent inputs it's going to be obtained the set 11…1, which blocs all the ways through the circuit, unsolvable situation for the test generation.

b) Even parity for some inputs and odd parity for the rest of the inputs.

In this case at some of the inputs of the convergent gate will have the value 0 and others 1, which leads to unsolvable logic conflicts. In the case of the 0 signal on the initial connection the situation remains with a problem.

On the other side, in the case of the convergent fan-out with opposed parity it can't be obtained the combination of the values 00…0 or 11…1. This situation signifies, in the case of the AND, NAND gates the impossibility for the detection of the error types 1→0 at all the inputs of the gate, and in the OR, NOR type of gates – the impossibility of detecting 0→1 type of error at all the inputs of the gate.

In the case that the parities are of the same kind at the inputs of the convergent gate, can be obtained only the values of the sets 00…0 or 11…1, and that means that in the AND, NAND type of gates the impossibility of detecting 0→1 type of error, and in the OR, NOR type of gates the 1→0 type of error. These situations appear because of the logical properties of the convergent gates.

In the case when the level of the logic signal on the initial connection is in the opposite form (has the value 0) the parity of the inputs at the convergent gate won't change,

Table 1. The parity of the convergent fan-out signals for the counterexample Schneider

but the apparition of the signals in the negative form will have the respective effect depending of the convergent logic gate.

These are the theoretic aspects of the problem and it is possible to represent artificial cases, foreign to the digital structures correctly built. In practice, to not have bad situations, any digital structure used in the testing process, must pass obliged through a thorough process of synthesis of the DC with a detailed checkup of the correctness minimization made and not admitting under no circumstances of the logic redundancy.

3. PARITY ANALYSIS OF THE CONVERGENT FAN-OUT SIGNALS FOR A DC OF A SCHNEIDER COUNTEREXAMPLE

The testability analysis for a DC of Schneider counterexample, which was effected in [5] established that, all the ways from each fan-out point A, B, C, D to the convergent gate pass, in some cases through an odd number of logic gates, which can represent possible dangers of unsolvable logic conflicts. The structural analysis takes in consideration only the number of logic gates through which the signal is propagated, but doesn't care about the presence of the inverters. More specific, the number of inversions on the propagation way of the signal represents the parity. It's going to be marked with p_p – even parity, and with p_i – odd parity of a signal for one way.

The results of the parity analysis of the way signals from the fan-out points A, B, C and D to the input of the convergent gate 12, of the Schneider counterexample are presented in table 1.

These results aren't totally adequate, because:

1) At all the primary inputs have been applied direct values of the signals;
2) The digital circuit of the Schneider counterexample may be an artificial one or obtained through contradictory classic procedures of synthesis;
3) The digital circuit of the Schneider counterexample may represent o special logic function.

IV. CONCLUSIONS

1. The parity analysis of the fan-out signals for a DC counterexample shows the presence at the inputs of the convergent gate for the logic signals with opposed parity, which indicates the possibility of apparition for the unsolvable logic conflicts.
2. The circuit for the Schneider counterexample represents an artificial circuit based on a specific logic function.
3. The parity analysis reflects the logic and functional properties of the circuit. To drag a more fondamental conclusion regarding the testability of the counterexample Schneider circuit it is necessary a more profound analysis of the properties of these circuit.
4. Only a more thoroughly analysis of the structural and functional particularities of the Schneider counterexample DC, may point out the correctness of the synthesis procedure for this digital structure.

BIBLIOGRAPHY

1. Roth J. P. Diagnosis of Automata Failures: A calculus and A Method. - IBM Journal of Research and Development, vol. 10, p. 278-291, 1966.
2. Schneider P. R. Counterexample On the Necessity to Examine D-Chains in Diagnostic Test Generation – An exemple, IBM Journal of Research and Development, vol. 11, No.1, p. 114-115, 1967.
3. Roth J. P., Bouricius W. G., Schneider P. R. Programmed Algorithms to Compute Tests to Detect and Distinguish Between Failures in Logic Circuits. - IEEE Trans. On Electronic Computers, vol. EC-16, No. 5, p. 567-579, 1967.
4. Chang H. Y., Manning E., Metze G. – Fault diagnosis of digital systems. – Wiley-Interscience, New York, London, Sydney, Toronto, 1970.
5. Cojocaru I. The testability estimation for the digital circuit of the Schneider counterexample. - Next to be published